film between the rows of sprocket holes, said through holes arranged relative to one another in said array at a pitch *p* and continuously along and transversely across said film.

REMARKS

Reconsideration of the above-referenced application in view of the following amendments and remarks is respectfully requested.

Claims 5-19 are pending in this case. Claims 5, 8, 9, 12, 14, 15, and 17 have been amended to better define the scope of the claimed invention.

Claims 5 and 6 stand rejected under 35 U.S.C. 102(b) as being anticipated by applicant's admitted prior art. Claim 5, as amended, includes the step of "forming a two-dimensional array of through holes in said insulation film between the rows of sprocket holes, each through hole in said array spaced from adjacent through holes by a pitch *p*." Applicant's admitted art does not include such a step. Therefore, Applicant respectfully submits that Claims 5 is patentable. Support for the amendment can be found, for example, in Figures 2 and 3 of the instant specification. Claim 6 depends from Claim 5 and is therefore patentable over the admitted art for at least the reasons presented above.

Claims 7, 8, and 12 stand rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Cho. Claims 7 and 8 depend from Claim 5. Claim 12 depends from Claim 9. Both Claims 5 and 9 includes the step of "forming a two-dimensional array of through holes in said insulation film between the rows of sprocket holes, each through hole in said array spaced from adjacent through holes by a pitch *p*." Neither Applicant's admitted art nor Cho teach or suggest such a step. Therefore, Applicant

respectfully submits that Claims 5 and 9 are patentable over the cited combination of references. Claims 7, 8, and 12 depend from Claims 5 and 9 and are therefore patentable for at least the reasons presented above.

Claim 9 stands rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art. Claim 9 includes the step of "forming a two-dimensional array of through holes in said insulation film between the rows of sprocket holes, each through hole in said array spaced from adjacent through holes by a pitch *p*." Applicant's admitted art does not include or suggest such a step. Therefore, Applicant respectfully submits that Claim 9 is patentable over the admitted art. Claim 10 depends from Claim 9 and is therefore patentable over the admitted art for at least the reasons presented above.

Claims 14, 15, 17, and 19 stand rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Cho. Claim 14, as amended, includes the step of "providing an insulation film having rows of sprocket holes at a pitch *L* along the edges of said film and a two-dimensional array of through holes in said film between the rows of sprocket holes, said through holes arranged relative to one another in said array at a pitch *p*." Neither Applicant's admitted art nor Cho teach or suggest such a step. Therefore, Applicant respectfully submits that Claim 14 is patentable over the cited combination. Claims 15, 17 and 19 depend from Claim 14 and are therefore patentable over the cited combination for at least the reasons presented above.

Claim 18 stands rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art and Cho and further in view of Hashimoto (U.S. Patent No. 6,200,824). Claim 18 depends from Claim 14, which is patentable over the combination of applicant's art with Cho for at least the reasons presented above. Hashimoto does not cure the deficiency of applicant's art and Cho with respect to Claim 14. In view of the dependency of Claim 18

from Claim 14, Applicant respectfully submits that Claim 18 is patentable over the cited combination for at least the reasons presented above.

Applicant thanks the Examiner for indicating the allowability of Claims 11, 13, and 16, but, in view of the arguments above regarding the claims from which Claims 11, 13, and 16 depend, Applicant respectfully declines to rewrite these claims at this time.

In view of the above, Applicant respectfully requests the entry of this amendment, the withdrawal of the Examiner's rejections, and allowance of Claims 5-19. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

5. (twice amended) A method for manufacture of an insulation film for providing an insulation substrate for carrying a semiconductor chip of a semiconductor package comprising the steps of:

providing an insulation film having two rows of sprocket holes comprising a plurality of sprocket holes formed at a pitch *L* along both edges of the insulation film; and

forming a two-dimensional array [plurality] of through holes in said insulation film [at a pitch *p*] between the rows of sprocket holes, each through hole in said array spaced from adjacent through holes by a pitch *p*.

8. (twice amended) The method for manufacture of an insulation film according to claim 6 wherein the method further comprises a step of forming a two-dimensional array [plurality] of circuit patterns upon the insulation film according to size of the semiconductor package and a for-plating-electricity-supply-use conductor pattern electrically connected with the array [plurality] of circuit patterns.

9. (twice amended) A method for manufacture of a semiconductor package comprising the steps of: providing an insulation film, forming two rows of sprocket holes comprising a plurality of sprocket holes formed at a pitch *L* along both edges of the insulation film, forming a two-dimensional array [plurality] of through holes [at a pitch *p*] between the rows of sprocket holes, each through hole in said array spaced from adjacent through holes by a pitch *p*, forming a two-dimensional plurality of circuit patterns upon the insulation film according to size of the semiconductor package, forming a for-plating-electricity-supply-use conductor pattern electrically connected with the plurality of circuit patterns having a main line surrounding a perimeter of the plurality of circuit patterns and a sub-line electrically connecting each of the circuit patterns to the main line;

mounting a semiconductor chip within a respective prescribed region of each circuit pattern of the insulation film and electrically connecting the semiconductor chip with the circuit pattern;

performing resin sealing for partitioning off each region enclosed by the main line of the conductor pattern; and

cutting apart into individual semiconductor packages by dicing along the sub-lines of the insulation film.

12. (twice amended) The method for manufacture of an insulation film according to claim 7 wherein the method further comprises a step of forming a two-dimensional array [plurality] of circuit patterns upon the insulation film according to size of the semiconductor package and a for-plating-electricity-supply-use conductor pattern electrically connected with the plurality of circuit patterns.

14. (amended) A method of packaging a semiconductor device, comprising the steps of:

providing an insulation film having rows of sprocket holes at a pitch *L* along the edges of said film and a two-dimensional array [plurality] of through holes in said film between the rows of sprocket holes, said through holes arranged relative to one another in said array at a pitch *p*;

mounting a semiconductor chip over a number of said through holes;

sealing said semiconductor chip and a portion of said insulation film in resin; and

cutting said insulation film surrounding said semiconductor chip to release said resin-sealed chip from the remainder of said insulation film.

15. (amended) The method of Claim 14, wherein said step of providing an insulation film comprises:

providing an insulation film having rows of sprocket holes at a pitch L along the edges of said film, and a two-dimensional array [plurality] of through holes in said film between the rows of sprocket holes, said through holes

arranged relative to one another in said array at a pitch *p* and continuously along and transversely across said film within circuit pattern regions on said film.

17. (amended) The method of Claim 14, wherein said step of providing an insulation film comprises:

providing an insulation film having rows of sprocket holes at a pitch L along the edges of said film, and a two-dimensional array [plurality] of through holes in said film between the rows of sprocket holes, said through holes arranged relative to one another in said array at a pitch *p* and continuously along and transversely across said film.